# Low Thermal Budget Monolithic Integration of Evanescent-Coupled Ge-on-SOI Photodetector on Si CMOS Platform

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***Abstract*—The design and fabrication of a monolithically integrated evanescent-coupled Ge-on-silicon-on-insulator (SOI) photodetector and CMOS circuits were realized on common SOI platform using an "electronic-first and photonic-last" integration approach. High-performance detector with an integrated Si waveguide was demonstrated on epitaxial Ge-absorbing layer selectively grown on an ultrathin SOI substrate. Performance metrics of photodetector designs featuring vertical and lateral PIN configurations were investigated. When operated at a bias of $-1.0$ V, a vertical PIN detector achieved a lower $I_{\rm dark}$ of $\sim$0.57 $\mu$A as compared to a lateral PIN detector, a value that is below the typical $\sim$1 $\mu$A upper limit acceptable for high-speed-receiver design. Very high responsivity of $\sim$0.92 A/W was obtained in both detector designs for a wavelength of 1550 nm, which corresponds to a quantum efficiency of $\sim$73%. Impulse response measurements showed that the vertical PIN detector gives rise to a smaller full-width at half-maximum of $\sim$24.4 ps over a lateral PIN detector, which corresponds to a $-3$ dB bandwidth of $\sim$11.3 GHz. *RC* time delay is shown to be the dominant factor limiting the speed performance. Eye patterns (pseudorandom binary sequence $2^7-1$) measurement further confirms the achievement of high-speed and low-noise photodetection at a bit rate of 8.5 Gb/s. Excellent transfer and output characteristics have also been achieved by the integrated CMOS inverter circuits in addition to the well-behaved logic functions. The introduction of an additional thermal budget (800 °C) arising from the Ge epitaxy growth has no observable detrimental impact on the short-channel control of the CMOS inverter circuit. In addition, we describe the issues associated with monolithic integration and discuss the potential of Ge-detector/Si CMOS receiver for future optical communication applications.**

***Index Terms*—CMOS circuit, germanium, integrated photonics, near infrared, photodetector, silicon-on-insulator (SOI).**

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## I. Introduction

THE CONVERGENCE of electronic–photonic integrated circuit is becoming increasingly important to keep up with the performance roadmap known as Moore's law [1]. Today, data transmissions at a bit rate of 10 Gb/s over long distance makes photonic interconnection an easier approach to implement than electrical interconnect. At this data rate, the conventional copper solution has begun to encounter extreme challenges related to power consumption and reach [2]. Pushing every gigabits of data through these copper wires has become much more expensive and complicated as it requires sophisticated techniques to overcome the distortion caused by the imperfection in the copper lines. Moreover, the growing issues in electromagnetic interference, signal crosstalk, and heavier weight make it an inferior approach for high-bandwidth applications [3]. To keep up with the scaling of interconnect bandwidth, an alternative solution makes use of optical interconnect technology to address the ever increasing bit rate requirement of data communication. However, the cost and form factor of conventional high-speed optical devices have been the major showstopper to the introduction of this technology for short-reach interconnect applications.

Over the past decades, conventional optical components were typically made of exotic III–V compound materials such as gallium arsenide (GaAs) and indium phosphide (InP) due to their excellent light emission and absorption properties. Unfortunately, compound-semiconductor devices are generally too complicated to process and costly to implement in optical interconnects. In search for a cost-effective solution, Si photonic emerges to hold great promise for its inexpensive material and its compatibility with current CMOS fabrication technology [4]. Recent advancements have also shown that silicon (Si) is a viable optical material suitable for high-bandwidth data communication applications. In addition, the feasibility of converging photonic and electronic integrated circuits (EPICs) all on a single chip makes it an extremely attractive option to extend the performance roadmap as driven by Moore's Law [1], [5].

However, to make silicon photonic communication a reality, several key technological challenges have to be addressed. Inferior optical properties of Si [6] have thus far the major showstopper to preclude the development of a key active photonic component needed for near-infrared optical detections. Very recently, Ge has attracted growing interest for the realization of high-performance photodetector [7]–[17] due to its large absorption coefficient [18] and its pseudodirect bandgap property.

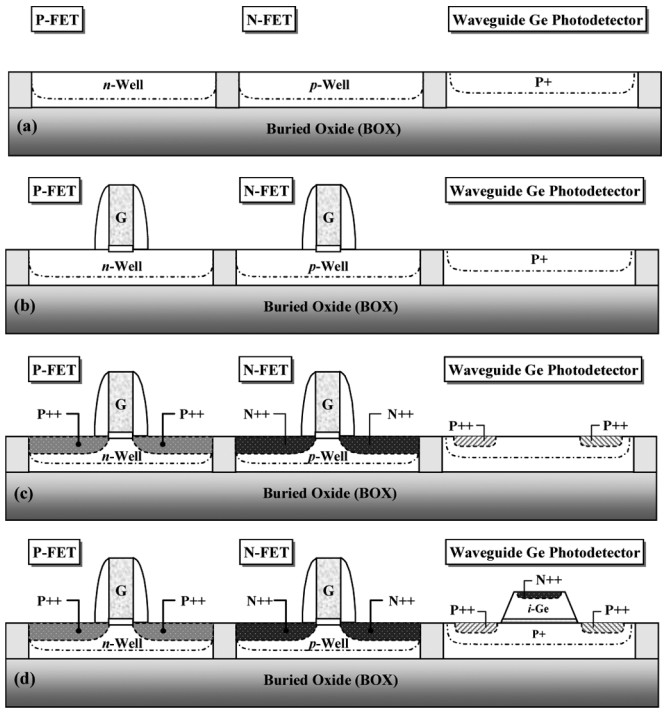


Fig. 1. Schematic showing the "electronic-first and photonic-last" integration approach for monolithically fabricating the evanescent-coupled Ge p-i-n photodetector and Si CMOS circuit on common SOI platform.

However, Ge can be a challenging material to integrate in a CMOS environment for its low thermal budget constraint and its large lattice mismatch of ∼4.2% with Si [19]. High defect densities seen in the Ge-on-silicon-on-insulator (SOI) epitaxial film could induce unfavorable carrier recombination process that would degrade the detector's performance.

In this paper, we describe our design and fabrication strategy toward realizing a monolithically integrated Ge photodetector and CMOS circuits on common SOI platform for high-speed receiver applications. The approach, based on the Ge-on-SOI technology, enables the realization of high-sensitivity and low-noise photodetector that is capable of performing efficient optical-to-electrical encoding in the near-infrared wavelengths regime. We explore photodetector designs with both vertical and lateral PIN configurations and elucidate the merits of these devices in terms of their dark current, responsivity, and bandwidth performance. In addition, we evaluate the dc characteristics of the monolithically fabricated CMOS inverter circuit. We assess the impact of the additional thermal budget arising from the Ge epitaxy growth on the threshold voltage variation of short-channel CMOS transistors and discuss the issues and potential for seamless integration of electronic and photonic integrated circuits.

## II. Device Fabrication and Material Characterization

Fig. 1 shows the "electronic-first and photonic-last" integration approach adopted for monolithically fabricating the Ge photodetector and CMOS integrated circuit on common SOI platform. Starting SOI substrate with a thin overlying Si layer thickness of ∼220 nm and a buried oxide thickness of ∼2 $\mu$m was used. Channel waveguide with a width of ∼200 nm was first formed by using the same Si mesa isolation process employed for proper electrical isolation. A good control of the sidewall profile was achieved for enabling low waveguide transmission loss. Using a thin sacrificial oxide, selective ion implantations were first performed to define the p-well and n-well regions of the n-MOS and p-MOS transistors, respectively [see Fig. 1(a)]. A moderately high p-type doping was also implanted on the detector's active region, in which the dose was carefully chosen to allow low series resistance while not impacting the quality of the as-grown Ge epitaxy film. Rapid thermal annealing at 1030 °C for 5 s was used to activate the dopant. After removing the sacrificial oxide, a thin gate oxide of ∼50 Å was formed by thermal oxidation and a low-pressure chemical vapor deposition (LPCVD) polysilicon of ∼100 nm was deposited and patterned to form the transistor gate electrodes [see Fig. 1(b)]. A thin sidewall spacer made of conformal oxide was deposited and followed by an anisotropic reactive ion etch. Deep source/drain implants for p++ and n++ regions were subsequently performed for the CMOS transistors and rapid thermal annealing at 1030 °C for 5 s was employed to activate the dopant. Simultaneously, the bottom contact of the Ge photodetector was also formed using a highly doped p++ region [see Fig. 1(c)]. A plasma-enhanced chemical vapor deposition (PECVD) passivation oxide layer of ∼600 Å was then deposited and patterned to open the Ge active window. Selective epitaxial growth of Ge was performed in an ultrahigh vacuum chemical vapor deposition (UHVCVD) epitaxy reactor. The selective Ge epitaxy process commenced with the deposition of a 20-nm silicon–germanium (SiGe) buffer and a 30 nm pure Ge seed layer. This was followed by the low-temperature Ge epitaxy performed at 550 °C [20]. High-quality Ge epitaxial film with a thickness of ∼500 nm was selectively grown on the detector's active region to form the absorbing layer for near-infrared wavelengths detections. A Ge surface roughness of ∼0.35 nm was measured using atomic force microscopy (AFM) and a dislocation defects density on the order of $\sim 10^7$ cm$^{-2}$ was determined using the etch-pit density (EPD) approach. The achievement of such low defects density is predominantly due to the insertion of a thin SiGe buffer layer grown using a low temperature approach. This is so because the low-temperature SiGe buffer plays a role in providing Ge dangling bonds as nucleation sites to ease the selective Ge epitaxy process. Moreover, such SiGe buffer also acts as an additional interface to relieve the large lattice mismatch strain of ∼4.2% between the Ge and the Si substrate [21]. As a result of such low defects level within the Ge film, postepitaxy Ge anneal was skipped to reduce the thermal budget.

High dose selective phosphorous implant was then performed and annealed at 500 °C for 5 min to form good n-type ohmic contact for the Ge detector. Following passivation oxide deposition, contact and metallization were subsequently done to complete the device fabrication. The SEM images of the Si CMOS circuit and the monolithically integrated Ge p-i-n photodetector were shown in Fig. 2(a) and (b), respectively. Transmission electron microscopy (TEM) micrograph of the completed Ge detector is shown in Fig. 3(a). The insertion of a SiGe buffer layer reduces the lattice mismatched between Ge and the Si substrate, which

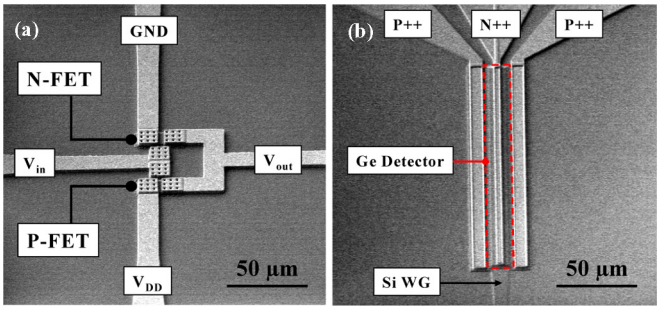


Fig. 2. (a) SEM micrograph of a Si CMOS inverter circuit on SOI platform. Partially depleted CMOS transistors with an effective channel length of ~180 nm were fabricated. (b) SEM micrograph of a monolithically integrated Ge p-i-n photodetector with a Si photonic waveguide.

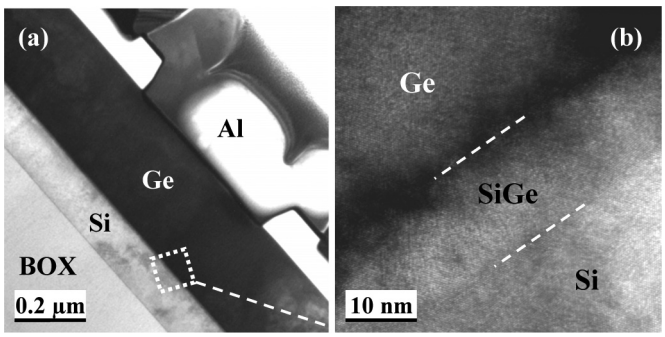


Fig. 3. (a) TEM micrograph of the completed Ge p-i-n photodetector. (b) High-resolution TEM image showing the insertion of SiGe buffer layer to reduce the lattice-mismatched between Ge and Si substrate.

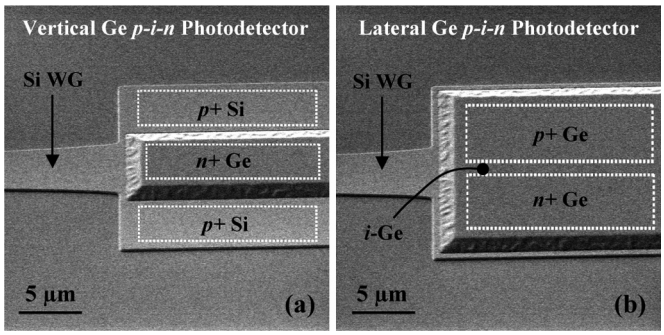


Fig. 4. (a) SEM micrograph showing the design of an evanescent coupled Ge photodetector featuring vertical p-i-n configuration. The width $W$ and length $L$ of the detector is 8 and 100 $\mu$m, respectively. (b) Ge photodetector design with a lateral p-i-n configuration. The width $W$ and length $L$ of this detector is 20 and 100 $\mu$m, respectively.

enables a low defect density Ge film to be epitaxially grown [see Fig. 3(b)].

## III. Germanium-on-SOI Photodetectors

### A. Evanescent-Coupled Ge-on-SOI Detector Designs

Fig. 4 shows the designs of the evanescent coupled Ge-on-SOI photodetectors employed in this study. Detectors featuring vertical and lateral PIN configurations were fabricated. For a vertical PIN detector, the p+ and n+ junctions were formed on the Si and Ge regions, respectively, with an intrinsic Ge absorbing layer

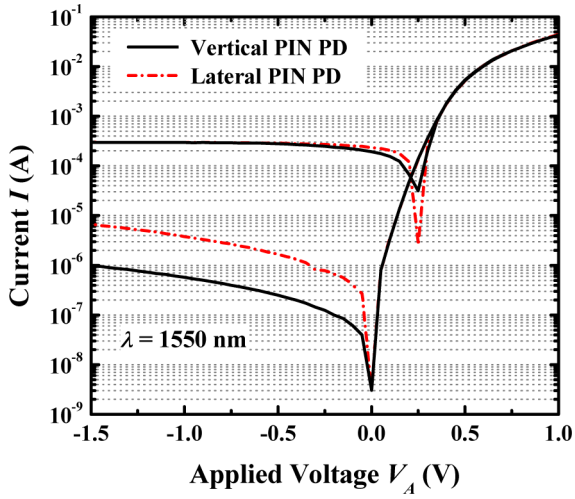


Fig. 5. The current–voltage characteristics of the vertical and lateral Ge p-i-n detectors under dark and illumination conditions. At a bias of −1.0 V, the vertical detector demonstrated a dark current of ~0.57 $\mu$A, which is below the 1 $\mu$A that is generally considered to be the upper limit for high-speed receiver design.

having a thickness of ~0.4 $\mu$m sandwiched in between these alternating junctions [see Fig. 4(a)]. The width $W$ and length $L$ of the vertical PIN detector is 8 and 100 $\mu$m, respectively. Such PIN design is often preferred over the metal-semiconductor-metal (MSM) structure as it enables the achievement of low leakage current. In this design, high absorption coefficient of the Ge layer allows the absorbing region to be kept very thin, while leverages on the detector length to improve the photodetection efficiency. In another detector design featuring lateral PIN configuration, both the $p^+$ and $n^+$ junctions were formed on the Ge region, and were separated by an intrinsic absorbing layer of ~0.8 $\mu$m [see Fig. 4(b)]. Note that the width $W$ and length $L$ of the lateral PIN detector is 20 and 100 $\mu$m, respectively. As a result of the difference in the refractive index between Si and Ge, the incident photon traveling in the Si waveguide will be evanescent-coupled into the Ge absorbing layer to enable optical-to-electrical encoding. In this context, the insertion of a thick buried oxide (BOX) serves as a cladding to confine the optical mode within the core of the channel waveguide so as to prevent leakage into the underneath Si substrate. The performance metric of these detectors will be investigated in the subsequent sections.

### B. Detector's DC Characteristics

Fig. 5 shows a plot of the current versus applied bias for both the vertical and lateral PIN detectors under dark and illumination conditions. All devices were observed to demonstrate excellent rectifying characteristics, showing a forward-to-reverse current ratio of ~4 orders of magnitude. At a given applied bias of −1.0 V, the dark current was measured to be ~0.57 $\mu$A (or ~ 0.7 nA/$\mu$m$^2$) in a vertical PIN detector, which is below the typical 1.0 $\mu$A generally considered to be the upper limit for high-speed receiver design. However, for a lateral PIN detector, a higher dark current of ~3.8 $\mu$A (or ~1.9 nA/$\mu$m$^2$) was

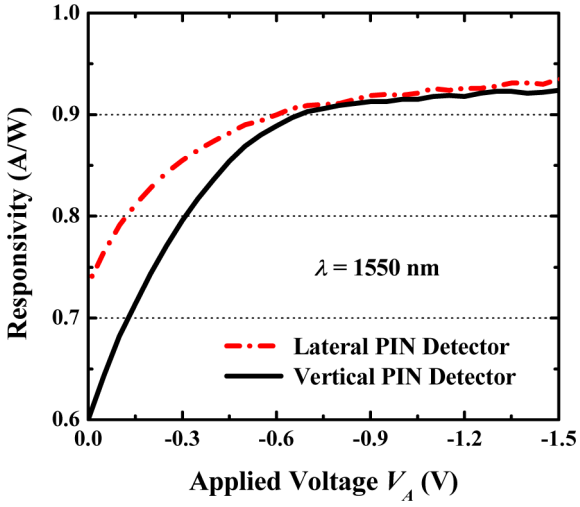


Fig. 6. Responsivity as a function of applied voltage measured at 1550 nm for both the lateral and vertical configured Ge photodetectors. Comparable responsivity performance was achieved in both the devices at a typical applied bias of −1.0 V.

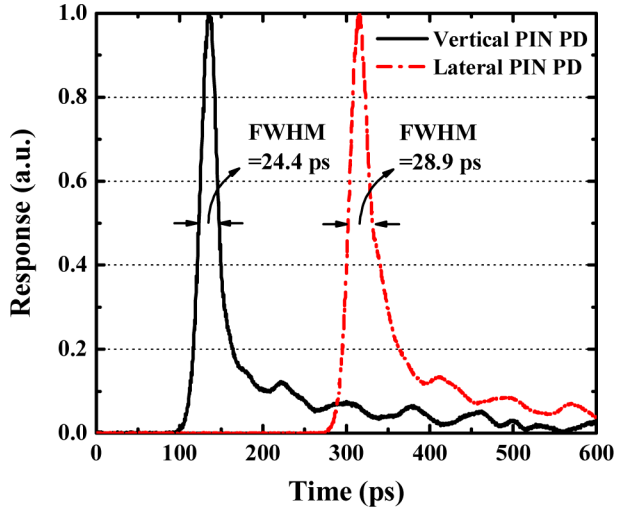


Fig. 7. Impulse response of the Ge-on-SOI photodetectors with vertical and lateral p-i-n configurations measured at an applied bias of −1.0 V and wavelength λ = 1550 nm. A vertical detector demonstrated a smaller FWHM pulsewidth of ∼24.4 ps as compared to a lateral detector, which corresponds to a –3 dB bandwidth of ∼11.3 GHz.

obtained. In order to compare their responsivity performance, optical measurements were performed by injecting an incident photon with a wavelength of 1550 nm into the Si waveguide and coupled to the overlying Ge absorbing layer for detection. The typical optical transmission loss in our Si waveguide is ∼2 dB/cm, and the light polarization is in TE mode. No coupler was integrated with the Si waveguide, and the incident light was coupled through a single-mode lensed fiber directly into the Si nanotaper. As such, high coupling loss of 3 dB ± 1 dB is not all unexpected. However, such loss performance could be further improved by integrating a coupler to enable efficient coupling of incident light into the Si waveguide. For an incident power of ∼300 $\mu$W, optical measurements showed that the detector achieved a photocurrent on the order of ∼275 $\mu$A, which was observed to saturate at higher biases.

Fig. 6 compares the responsivity of the detectors as a function of the applied voltages. It is interesting to note that the vertical PIN detector demonstrated a lower responsivity as compared to the lateral PIN detector for biases below −0.5 V. This could possibly be due to an enhanced carrier recombination process at the high density of defect centers near the Ge–Si heterojunction. This is set to compromise the absolute photocurrent value of a vertical PIN detector under low field influence. However, with an increased electrostatic potential across the junction, the photogenerated carriers will be assisted across the space charge region with enhanced mobility and be collected as photocurrent before they can recombine at these recombination centers. At an applied bias larger than −1.0 V, a comparable responsivity was measured for both the vertical and lateral PIN detectors. Despite that the metallurgical junction is separated by merely 0.8 $\mu$m, a lateral PIN detector showed a high absolute responsivity of ∼0.9 A/W. The possible mechanisms accountable for such high responsivity could be attributed to the following reasons. First, under high reversed bias, the intrinsic Ge region (i.e., between and beneath the metallurgical junction) was simulated to be totally depleted, as confirmed using MEDICI device simulator. When photon is absorbed to produce electron and hole pairs, the fringe field beneath the metallurgical junction enables the generated carriers to be collected by the electrode as photocurrent. Second, optical simulation shows that more than 80% of the incident light traveling in the waveguide is absorbed within the first 25 $\mu$m of the detector. Hence, by leveraging on the long absorption length design, nearly all incidence photons will be expected to contribute to the achievement of high responsivity.

### C. Pulse Response and Eye Pattern Measurements

Fig. 7 shows the impulse response of the vertical and lateral PIN detectors measured at a photon wavelength of 1550 nm. The measurement was performed with a 1.55-$\mu$m pulsed laser source having a 80 fs pulsewidth. Devices were characterized with microwave probes and the impulse response was captured using a sampling oscilloscope. A vertical PIN detector was shown to achieve a smaller full-width at half-maximum (FWHM) of ∼24.4 ps as compared to the lateral PIN detector with a slightly larger FWHM of ∼28.9 ps. This corresponds to a −3 dB bandwidth of ∼10.1 and ∼11.3 GHz, respectively, as obtained from the fast Fourier transform of the impulse response (not shown here). The detector's bandwidth can be further evidenced by the eye patterns measurements (pseudorandom binary sequence, PRBS $2^7$–1) done by directly connecting the output of the detector to the 50 Ω electrical input of the digital communications analyzer (DCA). Fig. 8 shows that high sensitivity and low-noise photodetection at a bit rate of 8.5 Gb/s can be achieved by the vertical PIN detector. This is in good agreement with our theoretical modeling results where *RC* time delay component is found to be the dominant factor limiting the bandwidth performance of a vertical PIN detector, as plotted in Fig. 9. It is noteworthy to mention that the total −3 dB bandwidth is defined by both the carrier transit and the

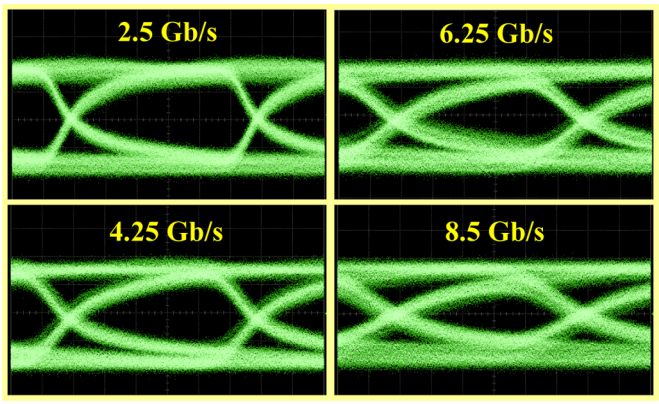


Fig. 8. Eye patterns (PRBS $2^7$–1) of the vertical detector measured at a bias of −1.0 V with different bit rates. The detector demonstrated high sensitivity and low-noise photodetection up to a bit rate of 8.5 Gb/s. The low noise property of the detector can be illustrated by the clean eye patterns.

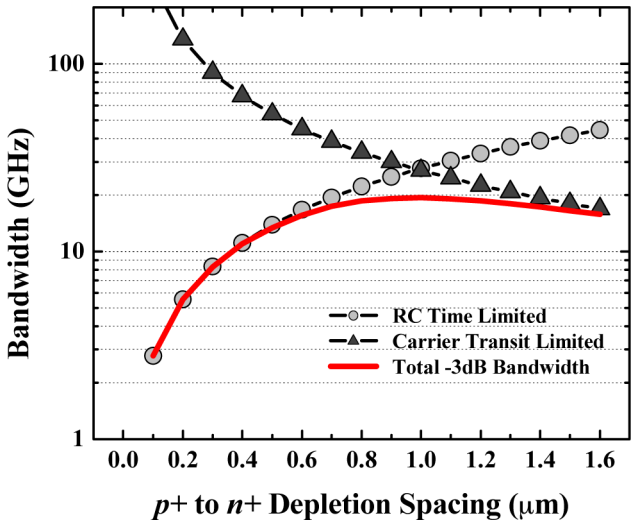


Fig. 9. Theoretical modeling showing the dependence of –3 dB bandwidth performance on the p+ to n+ depletion spacing.

*RC*-delay components that can be calculated using the following expressions:

$$f_{3\,\mathrm{dB}} = \sqrt{\frac{1}{1/f_{\mathrm{transit}}^2 + 1/f_{RC}^2}} \tag{1}$$

$$f_{\mathrm{Transit}} = \frac{0.45 v_{\mathrm{sat}}}{t_{i-\mathrm{Ge}}} \tag{2}$$

$$f_{RC} = \frac{1}{2\pi RC} \tag{3}$$

where $f_{\mathrm{Transit}}$ and $f_{RC}$ are the transit-limited and *RC*-limited bandwidth, respectively [22]. Higher speed measurements are possible through further scaling of detector geometry (i.e., length and width) to reduce the device capacitance and by downsizing the probe pads dimension for reduced parasitics.

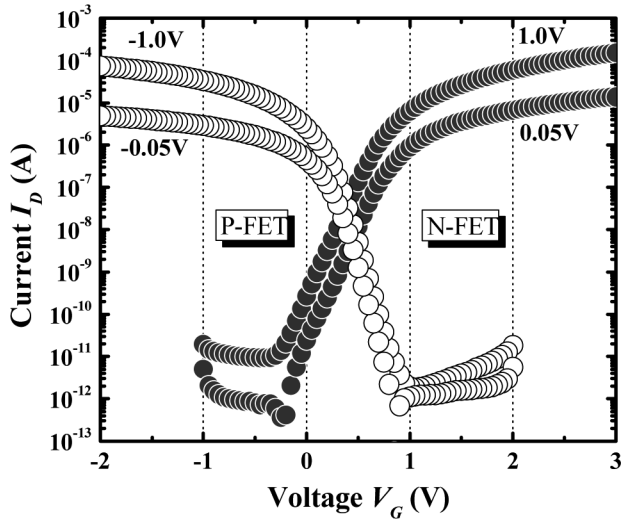


Fig. 10. Transfer characteristics of the n-MOS and p-MOS transistors connected in an inverter circuit, showing good control of short-channel effect.

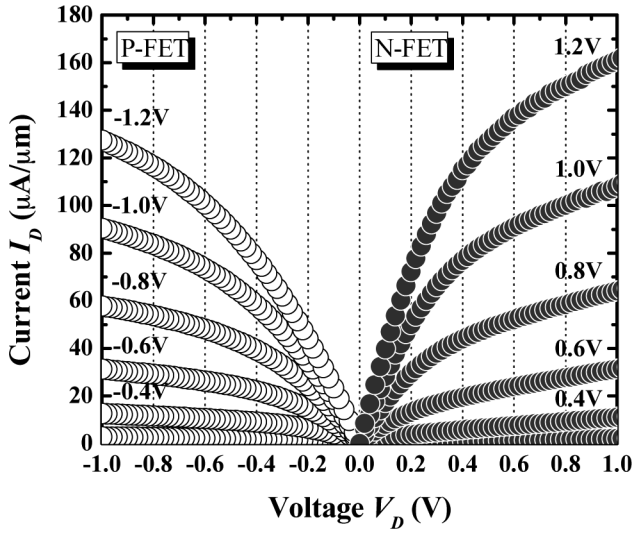


Fig. 11. Output characteristics ($I_{\mathrm{D}}$–$V_{\mathrm{D}}$) of the n-MOS and p-MOS transistors connected in an inverter circuit.

## IV. Integrated Si CMOS Circuit

### A. DC Characteristics of CMOS Transistors

This section discusses the dc characteristics of the monolithically integrated CMOS inverter circuit. Partially depleted CMOS transistors with an effective channel length of ∼180 nm were fabricated on thin SOI substrate. Fig. 10 plots the transfer characteristics ($I_{\mathrm{D}}$–$V_{\mathrm{G}}$) of the n-MOS and p-MOS transistors connected in an inverter circuit, showing a good control of short-channel effects. The drain-induced barrier lowering (DIBL) of the n-MOS and p-MOS devices were measured to be ∼0.2 and ∼0.11 V/V, respectively. Subthreshold swing of ∼166 and ∼120 mV/dec were also obtained. Fig. 11 shows the output characteristics ($I_{\mathrm{D}}$–$V_{\mathrm{D}}$) of the CMOS devices, showing a nearly comparable drain current. This was achieved through an approach to account for the mismatch in electron and hole mobility by choosing 3× longer device width for the p-MOS

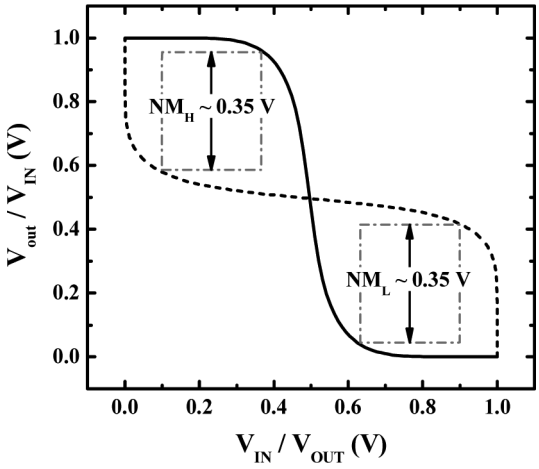


Fig. 12. Transfer curve of a matched inverter measured at a supply voltage $V_{\rm DD} = 1.0$ V with $V_{\rm IN}$ and $V_{\rm OUT}$ plotted interchangeably on $X$- and $Y$-axis. Good noise margin of ~0.35 V was achieved.

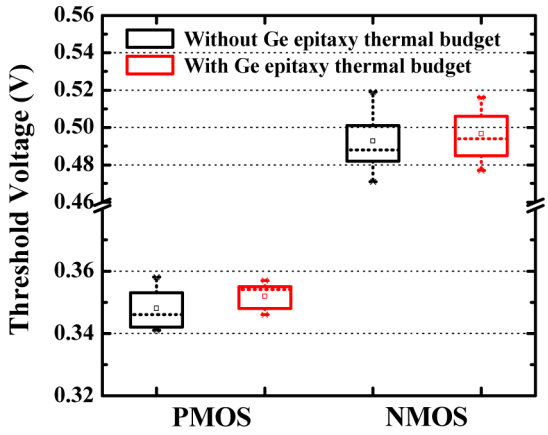


Fig. 13. Comparable threshold voltages were observed in both n-MOS and p-MOS transistors despite the introduction of an additional thermal budget during the Ge epitaxy growth. This enables Si CMOS to be monolithically fabricated with photonics devices for integrated receiver applications.

transistor. A matched inverter circuit will be extremely crucial to enable the achievement of symmetry in rise time and fall time during switching. Fig. 12 shows the transfer characteristics in butterfly shape for a matched inverter circuit, which simultaneously provides a good noise margin of ~0.35 V for a given supply voltage $V_{\rm DD}$ of 1.0 V.

### *B. Impact for Additional Thermal Budget on Short-Channel Characteristics of CMOS Transistors*

While an "electronic-first and photonic-last" integration approach was adopted, the impact of additional thermal budget on the CMOS short-channel characteristics deserves a careful investigation. This is important because any drift in the transistor's threshold voltage ($V_{\rm th}$) due to temperature-enhanced dopant diffusion would lead to severe impact on the circuit stability. High-temperature prebake process done at 800 °C for effective native oxide removal prior to the selective Ge epitaxy growth is one likely root cause to a possible $V_{\rm th}$ shift. This could give rise to concern for a degraded short-channel control. However, our experimental results show that despite the CMOS devices underwent the additional thermal budget, no observable detrimental impact on the threshold voltage was detected, as evidenced in Fig. 13. This can be seen from the nearly comparable short-channel characteristics demonstrated in both the n-MOS and p-MOS transistors, respectively. This shows the promise to enable the convergence of CMOS TIA/Ge-detector integrated circuit to allow small form factor and high-speed receiver applications.

### *C. Issues for Monolithic Integration*

High-performance electronic–photonic integrated circuits integration does not come without any technological challenges [23], [24]. Although it appears promising that an integration of Ge detectors paired with CMOS circuit is capable of meeting the performance requirements of high-speed receiver, several important integration issues have to be resolved before making it to reality. The major concern arises from the additional thermal budget as introduced by the Ge epitaxy growth. On one hand, high-temperature prebake treatment at 800 °C is necessary to allow high quality selective Ge epitaxy growth. On the other hand, such high-temperature process could potentially degrade the short-channel control of CMOS devices in advanced technology nodes where the physical gate length is expected to scale beyond 32 nm. It is worthy to mention that, in this study, no detrimental impact was experienced by the inverter circuit despite undergoing a high thermal budget process, which could possibly be due to a long effective channel length of ~180 nm. However, it should be emphasized that further geometrical scaling would render the high-temperature prebake treatment process to impose possible degradation to the short-channel control of aggressively scaled CMOS devices. Hence, the development of a lower temperature selective Ge epitaxy process will be critical to the successful implementation of a monolithic technology.

The second most pressing issue originates from the nonplanarity associated with the need for a thick Ge film deposition. This is particularly true for the integration of surface illuminated detectors for optical detection applications at both $\lambda = 1310$ and 1550 nm, where high responsivity can only be achieved with increasing Ge thickness. In this context, an Si waveguide geometry will be preferred as the requirement for thick absorption layer can be relaxed while leveraging on the detector length to enhance the photodetection efficiency. However, such waveguide structure introduces additional fiber-coupling loss and optical transmission loss that would reduce the quantum efficiency of the waveguide detectors. Current state-of-the-art fabrication technology is capable of enabling negligible Si waveguide transmission loss, but the fiber coupling and alignment associated with packaging remains a challenging task. Overcoming all these technological barriers would unleash the potential of Ge-detector/Si-CMOS-integrated receiver for future near-infrared optical communication applications.

## V. Conclusion

In conclusion, we have successfully realized a monolithic integration of evanescent-coupled Ge-on-SOI photodetector and

CMOS circuit on common SOI platform through an "electronic-first and photonic-last" integration approach. Highly efficient Ge p-i-n detector with an integrated Si photonic waveguide was demonstrated, showing an excellent responsivity and bandwidth performance of ∼0.92 A/W and ∼11.3 GHz, respectively. Vertical PIN detector design was found to offer a superior performance over a lateral PIN detector design in terms of bandwidth and dark current density. A closely matched inverter circuit was demonstrated, along with the achievement of good control of short-channel effects in the CMOS transistors. The introduction of an additional thermal budget imposes no detrimental impact on the threshold voltage variation in the CMOS devices. Process challenges and issues associated with the monolithic integration scheme were discussed. A seamless integration of electronic–photonic circuit is poised to become an enabling technology for future high-bandwidth on-chip optical interconnects application.

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## REFERENCES

[1] L. C. Kimerling, D. Ahn, A. B. Apsel, M. Beals, D. Carothers, Y. K. Chen, T. Conway, D. M. Gill, M. Grove, C.-Y. Hong, M. Lipson, J. Liu, J. Michel, D. Pan, S. S. Patel, A. T. Pomerene, M. Rasras, D. K. Sparacin, K.-Y. Tu, A. E. White, and C. W. Wong, "Electronic–photonic integrated circuits on the CMOS platform," *Proc. SPIE*, vol. 6125, p. 612502, 2006.

[2] K. Wada, H. C. Luan, D. R. C. Lim, and L. C. Kimerling, "On-chip interconnection beyond semiconductor roadmap-silicon microphotonics," *Proc. SPIE*, vol. 4870, pp. 437–443, 2002.

[3] C. Gunn, "CMOS photonics for high-speed interconnects," *IEEE Micro*, vol. 26, no. 2, pp. 58–66, Mar./Apr. 2006.

[4] R. Soref, "The past, present, and future of silicon photonics," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1678–1687, Nov./Dec. 2006.

[5] M. Beals, J. Michel, J. F. Liu, D. H. Ahn, D. Sparacin, R. Sun, C. Y. Hong, L. C. Kimerling, A. Pomerene, D. Carothers, J. Beattie, A. Kopa, A. Apsel, M. S. Rasras, D. M. Gill, S. S. Patel, K. Y. Tu, Y. K. Chen, and A. E. White, "Process flow innovations for photonic device integration in CMOS," *Proc. SPIE*, vol. 6898, pp. 689804-1–689804-14, 2008.

[6] R. A. Soref, "Silicon-based optoelectronics," *Proc. IEEE*, vol. 81, no. 12, pp. 1687–1706, Dec. 1993.

[7] L. Colace, G. Masini, and G. Assanto, "Ge-on-Si approaches to the detection of near-infrared light," *IEEE J. Quantum Electron.*, vol. 35, no. 12, pp. 1843–1852, Dec. 1999.

[8] G. Dehlinger, S. J. Koester, J. D. Schaub, J. O. Chu, Q. C. Ouyang, and A. Grill, "High-speed germanium-on-SOI lateral PIN photodiodes," *IEEE Photon. Technol. Lett.*, vol. 16, no. 11, pp. 2547–2549, Nov. 2004.

[9] M. Jutzi, M. Berroth, G. Wohl, M. Oehme, and E. Kasper, "Ge-on-Si vertical incidence photodiodes with 39-GHz bandwidth," *IEEE Photon. Technol. Lett.*, vol. 17, no. 7, pp. 1510–1512, Jul. 2005.

[10] S. J. Koester, J. D. Schaub, G. Dehlinger, and J. O. Chu, "Ge-on-SOI infrared detectors for integrated photonic applications," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1489–1502, Nov./Dec. 2006.

[11] M. Mike, D. Olufemi, S. Gadi, and C. Yoel, "Performance of Ge-on-Si p-i-n photodetectors for standard receiver modules," *IEEE Photon. Technol. Lett.*, vol. 18, no. 21, pp. 2442–2444, Dec. 2006.

[12] D. Ahn, C.-Y. Hong, J. F. Liu, W. Giziewicz, M. Beals, L. C. Kimerling, J. Michel, J. Chen, and F. X. Kartner, "High performance, waveguide integrated Ge photodetectors," *Opt. Express*, vol. 15, no. 7, pp. 3916–3921, Apr. 2007.

[13] Y. Tao, C. Rami, M. M. Mike, S. Gadi, C. Yoel, R. Doron, and M. J. Paniccia, "31 GHz Ge n-i-p waveguide photodetectors on silicon-on-insulator substrate," *Opt. Express*, vol. 15, pp. 13965–13971, Oct. 2007.

[14] K.-W. Ang, S. Zhu, M. Yu, G.-Q. Lo, and D.-L. Kwong, "High performance waveguided Ge-on-SOI metal–semiconductor–metal photodetectors with novel silicon–carbon (Si:C) Schottky barrier enhancement layer," *IEEE Photon. Technol. Lett.*, vol. 20, no. 9, pp. 754–756, May 2008.

[15] K.-W. Ang, S. Y. Zhu, J. Wang, K. T. Chua, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Novel silicon-carbon (Si:C) Schottky Barrier enhancement layer for dark current suppression in Ge-on-SOI MSM photodetectors," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 708–710, Jul. 2008.

[16] K.-W. Ang, M.-B. Yu, S.-Y. Zhu, K.-T. Chua, G.-Q. Lo, and D.-L. Kwong, "Novel NiGe MSM photodetector featuring asymmetrical Schottky barriers using sulfur Co-implantation and segregation," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 704–707, Jul. 2008.

[17] L. Chen, P. Dong, and M. Lipson, "High performance germanium photodetectors integrated on submicron silicon waveguides by low temperature wafer bonding," *Opt. Express*, vol. 16, pp. 11513–11518, 2008.

[18] J. M. Hartmann, A. Abbadie, A. M. Papon, P. Holliger, G. Rolland, T. Billon, J. M. Fedeli, M. Rouviere, L. Vivien, and S. Laval, "Reduced pressure—Chemical vapor deposition of Ge thick layers on Si(001) for 1.3–1.55-$\mu$m photodetection," *J. Appl. Phys.*, vol. 95, no. 10, pp. 5905–5913, May 2004.

[19] H.-C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, "High-quality Ge epilayers on Si with low threading-dislocation densities," *Appl. Phys. Lett.*, vol. 75, no. 19, pp. 2909–2911, Nov. 1999.

[20] K.-W. Ang, M.-B. Yu, G.-Q. Lo, and D.-L. Kwong, "Low voltage and high responsivity germanium bipolar phototransistor for optical detections in the near-infrared regime," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1124–1127, Oct. 2008.

[21] T. H. Loh, H. S. Nguyen, C. H. Tung, A. D. Trigg, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Ultrathin low temperature SiGe buffer for the growth of high quality Ge epilayer on Si(100) by ultra-high vacuum chemical vapor deposition," *Appl. Phys. Lett.*, vol. 90, pp. 092108-1–092108-3, Feb. 2007.

[22] M. Oehme, J. Werner, E. Kasper, M. Jutzi, and M. Berroth, "High bandwidth Ge p-i-n photodetector integrated on Si," *Appl. Phys. Lett.*, vol. 89, pp. 071117-1–071117-3, Aug. 2006.

[23] M. Salib, M. Morse, and M. Paniccia, "Opportunities and integration challenges for CMOS-compatible silicon photonic and optoelectronic devices," in *Proc. IEEE Int. Conf. Group IV Photon.*, Oct. 2004, pp. 1–3.

[24] M. Paniccia, A. S. Liu, N. Izhaky, and A. Barkai, "Integration challenge of silicon photonics with microelectronics," in *Proc. IEEE Int. Conf. Group IV Photon.*, Sep. 2005, pp. 20–22.

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